REMARKS

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa (U.S. Patent 5,933,436).

Claim 1 recites "ensuring that an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error, and passing the erroneous test data pattern as an output data value".

In contrast, Tanzawa teaches:

> After the correction of an error was conducted, a signal CORRECTi becomes high. However, in spite of the fact that a signal ERDETi informing that an error was detected became high, if the signal CORRECTi is still in a low state, i.e., in the case where no correction was conducted on an error, a signal NOTCORi becomes high." (Tanzawa, Col. 11, lines 7-12.)

The Examiner argues that this section of Tanzawa "is understood to mean that read data that is in error but cannot be corrected is output as is, uncorrected, as no arrangements for otherwise changing the data in error is disclosed".

It is initially noted that, contrary to the Examiner's assertions, the above-cited section of Tanzawa does not explicitly state that the error "cannot be corrected", but rather that "no correction was conducted on an error".

Moreover, the Applicant does not believe that above-cited section of Tanzawa must be understood as teaching that the "read data … is output as is, uncorrected" simply because "no arrangements for otherwise changing the data in error is disclosed". It is possible that the read data is simply not output at all when the high state of the NOTCORi

signal indicates that the read data contains an error. Otherwise, what is the benefit of generating the NOTCORi signal?

In addition, because Tanzawa explicitly teaches that a dedicated signal NOTCORi is generated to identify read data having an uncorrected error, there is no reason for Tanzawa to ensure "that an erroneous test data pattern having one or more error bits is provided" as recited by Claim 1. That is, because Tanzawa teaches that uncorrected errors are identified by a dedicated signal NOTCORi, Tanzawa does not need to ensure that the read data includes any errors, because the NOTCORi signal (and not the read data) identifies the presence of uncorrected errors.

In addition, Claim 1 recites "wherein the ECC values are not accessible from outside the semiconductor memory". The Examiner has not indicated where Tanzawa teaches that the ECC values are not accessible from outside the semiconductor memory.

For these reasons, Claim 1 is allowable over Tanzawa under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Tanzawa for at least the same reasons as Claim 1.

Claim 9, which recites "ensuring that an erroneous test data pattern having one or more error bits is provided if a multiple-bit error exists in the combination of a retrieved test data pattern and a corresponding ECC value, and passing the erroneous test data patterns as output data values, wherein the ECC values are not accessible from outside the semiconductor memory" is allowable over Tanzawa for reasons similar to Claim 1. Claims 11-17, which depend from Claim

9, are allowable over Tanzawa for at least the same reasons as Claim 9.

Claim 19, which recites "the memory interface does not provide direct access to the ECC values" and "a set of test data patterns associated with the semiconductor memory, wherein the set of test data patterns are selected such that any multiple-bit error in a combination including a test data pattern and a corresponding ECC value causes the error detection/correction unit to provide an output data pattern having an error, thereby rendering multiple-bit faults 100% detectable" is allowable over Tanzawa for reasons similar to Claim 1.

Claim 20, which recites "wherein the ECC values are not accessible from outside the semiconductor memory device" and "wherein the error detection/correction circuit is configured to … ensure that one or more error bits exist in the output test data pattern if a multiple-bit error exists in the combination of the test data pattern and the corresponding ECC value" is allowable over Tanzawa for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Tanzawa for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Shinoda et al. (U.S. Patent 5,177,743).

Claim 1 recites "ensuring that an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error, and passing the erroneous test data pattern as an output data value".

The Examiner admits that Shinoda et al. do not suggest changing uncorrectable data. Suppose that a test data pattern and a corresponding ECC value read from the memory array of Shinoda et al. included a multiple-bit error which existed entirely within the ECC value. If Shinoda et al. output the test data pattern without change, then Shinoda et al. would output a test data pattern having no error bits. Thus, by failing to suggest changing uncorrectable data, Shinoda et al. fail to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Shinoda et al. under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Shinoda et al. for at least the same reasons as Claim 1.

Claim 9, which recites "ensuring that an erroneous test data pattern having one or more error bits is provided if a multiple-bit error exists in the combination of a retrieved test data pattern and a corresponding ECC value, and passing the erroneous test data patterns as output data values" is allowable over Shinoda et al. for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Shinoda et al. for at least the same reasons as Claim 9.

Claim 19, which recites "the memory interface does not provide direct access to the ECC values" and "a set of test data patterns associated with the semiconductor memory, wherein the set of test data patterns are selected such that any multiple-bit error in a combination including a test

data pattern and a corresponding ECC value causes the error detection/correction unit to provide an output data pattern having an error, thereby rendering multiple-bit faults 100% detectable" is allowable over Shinoda et al. for reasons similar to Claim 1.

Claim 20, which recites "wherein the ECC values are not accessible from outside the semiconductor memory device" and "wherein the error detection/correction circuit is configured to … ensure that one or more error bits exist in the output test data pattern if a multiple-bit error exists in the combination of the test data pattern and the corresponding ECC value" is allowable over Shinoda et al. for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Shinoda et al. for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Shinoda et al. in view of Eaton et al. (U.S. Patent 4,939,694).

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Shinoda et al. The Examiner cites Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Shinoda et al. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Shinoda et al. in view of Eaton et al.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki (U.S. Patent 4,706,248).

The Examiner admits that Masaki (like Shinoda et al.) does not suggest changing uncorrectable data. Thus, like

Shinoda et al., Masaki necessarily fails to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Masaki under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Masaki for at least the same reasons as Claim 1.

Claim 9 is allowable over Masaki for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Masaki for at least the same reasons as Claim 9.

Claim 19 is allowable over Masaki for reasons similar to Claim 1.

Claim 20 is allowable over Masaki for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Masaki for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki in view of Eaton et al.

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Masaki. The Examiner cites Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Masaki. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Masaki in view of Eaton et al.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (U.S. Patent 4,726,021).

The Examiner admits that Horiguchi et al. (like Shinoda et al. and Masaki) do not suggest changing uncorrectable data. Thus, like Shinoda et al. and Masaki, Horiguchi et al. necessarily fail to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Horiguchi et al. under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Horiguchi et al. for at least the same reasons as Claim 1.

Claim 9 is allowable over Horiguchi et al. for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Horiguchi et al. for at least the same reasons as Claim 9.

Claim 19 is allowable over Horiguchi et al. for reasons similar to Claim 1.

Claim 20 is allowable over Horiguchi et al. for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Horiguchi et al. for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. in view of Eaton et al.

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Horiguchi et al. The Examiner cites

Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Horiguchi et al. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Horiguchi et al. in view of Eaton et al.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada (U.S. Patent 5,151,906).

The Examiner admits that Sawada (like Shinoda et al., Masaki and Horiguchi et al.) does not suggest changing uncorrectable data. Thus, like Shinoda et al., Masaki and Horiguchi et al., Sawada necessarily fails to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Sawada under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Sawada for at least the same reasons as Claim 1.

Claim 9 is allowable over Sawada for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Sawada for at least the same reasons as Claim 9.

Claim 19 is allowable over Sawada for reasons similar to Claim 1.

Claim 20 is allowable over Sawada for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are

allowable over Sawada for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of Eaton et al.

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Sawada. The Examiner cites Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Sawada. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Sawada in view of Eaton et al.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Drake et al. (U.S. Patent 5,535,226).

The Examiner admits that Drake et al. (like Shinoda et al., Masaki, Horiguchi et al. and Sawada) do not suggest changing uncorrectable data. Thus, like Shinoda et al., Masaki , Horiguchi et al. and Sawada, Drake et al. necessarily fails to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Drake et al. under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Drake et al. for at least the same reasons as Claim 1.

Claim 9 is allowable over Drake et al. for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Drake et al. for at least the same reasons as Claim 9.

Claim 19 is allowable over Drake et al. for reasons similar to Claim 1.

Claim 20 is allowable over Drake et al. for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Drake et al. for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Drake et al. in view of Eaton et al.

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Drake et al. The Examiner cites Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Drake et al. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Drake et al. in view of Eaton et al.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nozoe (U.S. Patent 6,549,460).

The Examiner admits that Nozoe (like Shinoda et al., Masaki, Horiguchi et al., Sawada and Drake et al.) does not suggest changing uncorrectable data. Thus, like Shinoda et al., Masaki , Horiguchi et al., Sawada and Drake et al., Nozoe necessarily fails to teach "ensuring than an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the

corresponding ECC value read from the memory array includes a multiple-bit error" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Nozoe under 35 U.S.C. 103(a).

Claims 2-6 and 8, which depend from Claim 1, are allowable over Nozoe for at least the same reasons as Claim 1.

Claim 9 is allowable over Nozoe for reasons similar to Claim 1. Claims 11-17, which depend from Claim 9, are allowable over Nozoe for at least the same reasons as Claim 9.

Claim 19 is allowable over Nozoe for reasons similar to Claim 1.

Claim 20 is allowable over Nozoe for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Nozoe for at least the same reasons as Claim 20.

Claims 1-6, 8, 9, 11-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nozoe in view of Eaton et al.

As described above, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Nozoe. The Examiner cites Eaton et al. for further support of the position that uncorrectable data is output unchanged. For this reason, Eaton et al. do not remedy the above-described deficiencies of Nozoe. Thus, Claims 1-6, 8, 9, 11-17 and 19-23 are allowable over Nozoe in view of Eaton et al.

Claims 1-17 and 19-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshinogawa (U.S. Patent 6,052,816).

The Examiner argues that Yoshinogawa teaches "uncorrectable data is purposefully changed by a 'different data generating circuit' (5)."

However, this statement is inaccurate. The Applicant is unable to identify any section of the Yoshinogawa that contemplates 'uncorrectable' data.

Yoshinogawa teaches that 'different data generating circuit 5' is controlled to reverse previously corrected data C to create incorrect data D if a verify mode is enabled. Yoshinogawa teaches that the correct data C is reversed to create incorrect output data D "only when an error exists either in the main data A or in the parity data B and the mode is the verify mode". (Yoshinogawa, Col. 3, lines 2-30.) Thus, Yoshinogawa teaches that in the verify mode, corrected data is purposefully reversed to create incorrect data, thereby enabling a failure to be detected.

For this reason, Yoshinogawa fails to teach or suggest "ensuring that an erroneous test data pattern having one or more error bits is provided if the combination of the test data pattern and the corresponding ECC value read from the memory array includes a multiple-bit error, and passing the erroneous test data pattern as an output data value" as recited by Applicant's Claim 1.

For these reasons, Claim 1 is allowable over Yoshinogawa under 35 U.S.C. 103(a).

Claims 2-8, which depend from Claim 1, are allowable over Yoshinogawa for at least the same reasons as Claim 1.

Claim 9 is allowable over Yoshinogawa for reasons similar to Claim 1. Claims 10-17, which depend from Claim 9, are allowable over Yoshinogawa for at least the same reasons as Claim 9.

Claim 19 is allowable over Yoshinogawa for reasons similar to Claim 1.

Claim 20 is allowable over Yoshinogawa for reasons similar to Claim 1. Claims 21-23, which depend from Claim 20, are allowable over Yoshinogawa for at least the same reasons as Claim 20.

CONCLUSION

Claims 1-17 and 19-23 are pending in the present application. Reconsideration and allowance of these claims is requested. If the Examiner has any questions or comments, he is invited to call the undersigned at (925) 895-3545.

Respectfully submitted,

/E. Eric Hoffman#38186/

Customer No.: 22888

E. Eric Hoffman
Attorney for Applicant
Reg. No. 38,186